**In the Claims:**

1. (currently amended) A leadframe for use with packaged integrated circuit chips comprising:

a leadframe having segments intended for solder attachment; and

gold selectively plated on said segments of said leadframe intended for solder attachment.

2. (previously presented) A leadframe for use with packaged integrated circuit chips having a chip mount pad and a plurality of lead segments, comprising:

a leadframe base made of copper or copper alloy;

a first layer of nickel deposited on said copper or copper alloy;

a layer of an alloy of nickel and palladium on said first nickel layer;

a second layer of nickel on said alloy layer, said second nickel layer deposited to be suitable for bending of said lead segments, wire bonding, and solder attachment;

a layer of palladium, said palladium layer deposited to be suitable for protecting the nickel surface for wire bonding and solderability, and for adhesion to molding compound; and

gold selectively plated on segments of said leadframe intended for solder attachment.

3. (previously presented) The leadframe according to Claim 2 wherein said gold layer has a thickness in the range from 2 to 5 nm.

4. (previously presented) The leadframe according to Claim 2 wherein said first nickel layer has a thickness in the range from 50 to 150 nm.

5. (previously presented) The leadframe according to Claim 2 wherein said alloy layer has a thickness in the range from 50 to 150 nm.

6. (previously presented) The leadframe according to Claim 2 wherein said second nickel layer has a thickness in the range from 1000 to 3000 nm.

7. (previously presented) The leadframe according to Claim 2 wherein said palladium layer has a thickness in the range from 25 to 75 nm.

8. (previously presented) The leadframe according to Claim 2 wherein said copper or copper alloy base has a thickness between about 100 and 250 μm.

9. (previously presented) The leadframe according to Claim 2 wherein said solder attachment comprises solder materials selected from a group consisting of tin/lead, tin/indium, tin/silver, tin/bismuth and conductive adhesive compounds.

10. (currently amended) The leadframe according to Claim 2 ~~1~~ wherein said leadframe comprises an iron-nickel alloy or invar base, selectively plated with gold.

11. (previously presented) A packaged semiconductor device comprising:

a leadframe comprising a chip mount pad for an integrated circuit chip and a plurality of lead segments having their first end near said mount pad and their second end remote from said mount pad;

said leadframe having a first surface layer of nickel, a layer of an alloy of nickel and palladium, a second layer of nickel, and a layer of palladium;

said leadframe further having gold selectively plated on segments of said leadframe intended for solder attachment;

an integrated circuit chip attached to said mount pad; and

bonding wires interconnecting said chip and said first ends of said lead segments.

12. (previously presented) The device according to Claim 11 wherein said bonding wires are selected from a group consisting of gold, copper, aluminum and alloys thereof.

13. (previously presented) The device according to Claim 11 wherein the bonding wire contacts to said first ends of said lead segments comprise welds made by ball bonds, stitch bonds, or wedge bonds.

14 to 22 (cancelled)

23. (previously presented) A packaged semiconductor device, comprising:

a leadframe comprising a chip mount pad for an integrated circuit chip and a plurality of lead segments;

said leadframe having a layer of nickel and a layer of palladium covering said chip mount pad and said plurality of lead segments, and gold selectively plated on portions of said lead segments intended for solder attachment;

an integrated circuit chip attached to said mount pad; and

bonding wires interconnecting said chip and said first ends of said lead segments.

24. (previously presented) A packaged semiconductor device, comprising:

a leadframe comprising a chip mount pad for an integrated circuit chip and a plurality of lead segments;

said leadframe having a layer of nickel and a layer of palladium covering said chip mount pad and said plurality of lead segments, and gold selectively plated on portions of said lead segments intended for solder attachment, wherein said layer of palladium has a thickness in the range of about 0.03% to about 6% of a thickness of said nickel layer;

an integrated circuit chip attached to said mount pad; and

bonding wires interconnecting said chip and said first ends of said lead segments.

25. (previously presented) The packaged semiconductor device of Claim 24, wherein said layer of nickel has a thickness in the range of about 500 nm to about 3000 nm and said palladium layer has a thickness in the range of about 10 nm to about 30 nm.

26. (previously presented) The packaged semiconductor device of Claim 24, wherein said gold has a thickness in the range of about 6% to about 50 % of said thickness of said palladium layer.